Amendment to the Claims:

1 (currently amended): A method of grouping cells for scan testing ~~in an integrated circuit design~~ comprising steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) initializing a corresponding list of cells for each of a plurality of ~~a~~ common signal domains ~~domain~~ in the integrated circuit design, each corresponding list of cells created as an empty list;

(c) selecting a cell that belongs ~~belonging~~ to one of the ~~a~~ common signal domains and ~~domain~~ that is not included in a corresponding list of cells for any of the ~~a~~ common signal domains ~~domain~~;

(d) tracing a net from an input port of the selected cell to a signal driver;

(e) inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver;

(f) tracing the net to an input port of each cell connected to the signal driver; and

(g) inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver.

2 (currently amended): The method of Claim 1 further comprising a step of repeating steps (c), (d), (e), (f), and (g) until every cell belonging to the ~~a~~ common signal domain associated with the signal driver has been inserted in the ~~a~~ corresponding list of cells for the common signal domain associated with the signal driver.

3 (currently amended): The method of Claim 2 further comprising a step of generating as output the ~~a~~ corresponding list of cells for each of the plurality of ~~a~~ common signal domains ~~domain~~ in the integrated circuit design.

4 (previously presented): The method of Claim 1 wherein step (e) includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver.

5 (currently amended): The method of Claim 1 comprising performing steps (b), (c), (d), (e), (f), and (g) for cells comprising ~~that are~~ flip-flops in a scan chain.

6 (currently amended): The method of Claim 5 comprising performing steps (b), (c), (d), (e), (f), and (g) for one of the ~~a~~ common signal domains ~~domain~~ that is a scan clock domain.

7 (previously presented): The method of Claim 6 comprising performing steps (d), (e), (f), and (g) for a net that is a clock net.

8 (previously presented): The method of Claim 7 comprising performing steps (d), (e), (f), and (g) for an input port that is a clock port.

9 (previously presented): The method of Claim 8 comprising performing steps (d), (e), (f), and (g) for a signal driver that is a clock driver.

10 (currently amended): A computer program product

for grouping cells ~~scan flops~~ for scan testing comprising[[:]] a computer readable medium ~~for~~ embodying a computer program for input to a computer, the[;]] ~~and a~~ computer program, when executed by the computer, ~~embodied in the medium for~~ causing the computer to perform steps of:

(a) receiving as input a representation of an integrated circuit design;

(b) initializing a corresponding list of cells for each of a plurality of ~~a~~ common signal domains ~~domain~~ in the integrated circuit design, each corresponding list of cells created as an empty list;

(c) selecting a cell that belongs ~~belonging~~ to one of the ~~a~~ common signal domains and ~~domain~~ that is not included in a corresponding list of cells for any of the ~~a~~ common signal domains ~~domain~~;

(d) tracing a net from an input port of the selected cell to a signal driver;

(e) inserting the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver;

(f) tracing the net to an input port of each cell connected to the signal driver; and

(g) inserting each cell traced from the net to an input port of the cell in the corresponding list of cells for the common signal domain associated with the signal driver.

11 (currently amended): The computer program product of Claim 10 further causing the computer to perform a step of repeating steps (c), (d), (e), (f), and (g) until every cell belonging to the ~~a~~ common signal domain associated with the signal driver has been inserted in the ~~a~~ corresponding list of cells for the common signal domain

associated with the signal driver.

12 (currently amended): The computer program product of Claim 11 further causing the computer to perform a step of generating as output the ~~a~~ corresponding list of cells for each of the plurality of ~~a~~ common signal domains ~~domain~~ in the integrated circuit design.

13 (previously presented): The computer program product of Claim 10 wherein step (e) includes storing a name of the selected cell in the corresponding list of cells for the common signal domain associated with the signal driver.

14 (currently amended): The computer program product of Claim 10 further causing the computer to perform steps (b), (c), (d), (e), (f), and (g) for cells comprising ~~that are~~ flip-flops in a scan chain.

15 (currently amended): The computer program product of Claim 14 further causing the computer to perform steps (b), (c), (d), (e), (f), and (g) for one of the ~~a~~ common signal domains ~~domain~~ that is a scan clock domain.

16 (previously presented): The computer program product of Claim 15 further causing the computer to perform steps (d), (e), (f), and (g) for a net that is a clock net.

17 (previously presented): The computer program product of Claim 16 further causing the computer to perform steps (d), (e), (f), and (g) for an input port that is a clock port.

18 (previously presented): The computer program product of Claim 17 further causing the computer to perform steps (d), (e), (f), and (g) for a signal driver that is a clock driver.